

## IN THE CLAIMS

The current claims for this application are listed below:

1. (Currently amended)      A method of forming a germanium-on-insulator (GOI) substrate comprising:
  - forming an epitaxial germanium layer on top of a first substrate;
  - forming a first dielectric film on top of the epitaxial germanium layer;
  - providing a second semiconductor substrate comprising a semiconductor surface;
  - bonding the first substrate directly to the second substrate by bonding the first dielectric film to the semiconductor surface of the second substrate, the bonding resulted in a bonded wafer pair; and
  - removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate.
2. (Canceled)
3. (Original)    A method as in claim 1 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.
4. (Original)    A method as in claim 1 further comprising:
  - polishing the surface of the first dielectric film prior to the bonding.
- 5-6. (Canceled)
7. (Previously Presented)      A method as in claim 1 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.
8. (Canceled)

9. (Original) A method as in claim 1 wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate.
10. (Original) A method as in claim 1 further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding.
11. (Original) A method as in claim 1 further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute.
12. (Currently amended) A method of bonding a germanium layer having a rough surface to a substrate comprising:
- forming an epitaxial germanium layer on top of a first substrate, the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS;
  - forming a first dielectric film on top of the rough surface;
  - bonding the first dielectric film directly to a semiconductor surface of a second semiconductor substrate, the bonding resulted in a bonded wafer pair wherein the first dielectric film is located between the epitaxial germanium layer and the second substrate; and
  - removing the first substrate after the bonding to expose epitaxial germanium layer.

13. (Canceled)

14. (Original) A method as in claim 12 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.
15. (Original) A method as in claim 12 further comprising:  
polishing the surface of the first dielectric film prior to the bonding.
- 16-18. (Canceled)
19. (Original) A method as in claim 12 wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate.
20. (Original) A method as in claim 12 further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding.
21. (Original) A method as in claim 12 further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute.
22. (Currently amended) A method of fabricating a semiconductor device comprising:  
forming an epitaxial germanium layer on top of a first substrate;  
forming a first dielectric film on top of the epitaxial germanium layer;  
providing a second semiconductor substrate comprising a semiconductor surface;  
bonding the first substrate directly to the semiconductor surface of the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair;

removing the first substrate after the bonding to expose epitaxial germanium layer to form a GOI substrate; and  
forming an electronic device on the GOI substrate.

23. (Original) A method as in claim 22 wherein the electronic device includes one of a transistor and a detector.

24. (Original) A method as in claim 23 wherein the transistor includes a gate dielectric, a gate electrode, spacers and source/drain regions.

25. (Original) A method as in claim 23 wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode.

26. (Canceled)

27. (Original) A method as in claim 22 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.

28. (Original) A method as in claim 22 further comprising:  
polishing the surface of the first dielectric film prior to the bonding.

29. (Canceled)

30. (Original) A method as in claim 22 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.

31-32. (Canceled)

33. (Currently Amended) A method of forming a germanium-on-insulator (GOI) substrate comprising:

forming an epitaxial germanium layer on top of a first substrate, the epitaxial germanium layer having a surface roughness;  
forming a first dielectric film on top of the epitaxial germanium layer, the first dielectric film sufficiently thick to cover the surface roughness of the epitaxial germanium layer;  
polishing the surface of the first dielectric film;  
providing a second substrate;  
bonding the first substrate to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair; and  
removing the first substrate after the bonding to expose epitaxial germanium layer to form the GOI substrate.

34. (Previously Presented) A method as in claim 33 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.

35. (Previously Presented) A method as in claim 33 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.

36. (Previously Presented) A method as in claim 33 wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate.

37. (Previously Presented) A method as in claim 33 further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding.

38. (Previously Presented) A method as in claim 33 further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute.
39. (Currently Amended) A method of bonding a germanium layer having a rough surface to a substrate comprising:
- forming an epitaxial germanium layer on top of a first substrate, the epitaxial germanium layer having a rough surface, the rough surface has a roughness value approximately greater than 2nm RMS;
  - forming a first dielectric film on top of the rough surface, the first dielectric film sufficiently thick to cover the surface roughness of the epitaxial germanium layer;
  - polishing the surface of the first dielectric film;
  - bonding the polished first dielectric film to a second substrate, the bonding resulted in a bonded wafer pair wherein the first dielectric film is located between the epitaxial germanium layer and the second substrate; and
  - removing the first substrate after the bonding to expose epitaxial germanium layer.
40. (Previously Presented) A method as in claim 39 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.
41. (Previously Presented) A method as in claim 39 wherein each of the first substrate and the second substrate semiconductor wafer is selected from a group consisting of a silicon (Si) substrate, a monocrystalline Si substrate, a polycrystalline Si substrate, a Si-containing substrate, a Si substrate having an oxide layer, a silicon-on-insulator (SOI) substrate, a gallium arsenide substrate, and Ge-containing substrate.

42. (Previously Presented) A method as in claim 39 further comprising causing a surface activation to the top surface of the first dielectric film and at least one surface of the second substrate to facilitate the bonding.
43. (Previously Presented) A method as in claim 39 further comprises annealing the bonded wafer pair at a predetermined annealing temperature, wherein the annealing temperature is achieved with a temperature ramp rate of approximately 1°C/minute.
44. (Currently Amended) A method of fabricating a semiconductor device comprising:  
forming an epitaxial germanium layer on top of a first substrate, the epitaxial germanium layer having a surface roughness;  
forming a first dielectric film on top of the epitaxial germanium layer, the first dielectric film sufficiently thick to cover the surface roughness of the epitaxial germanium layer;  
polishing the surface of the first dielectric film;  
providing a second substrate;  
bonding the first substrate to the second substrate by bonding the first dielectric film to the second substrate, the bonding resulted in a bonded wafer pair;  
removing the first substrate after the bonding to expose epitaxial germanium layer to form a GOI substrate; and  
forming an electronic device on the GOI substrate.
45. (Previously Presented) A method as in claim 44 wherein the electronic device includes one of a transistor and a detector.
46. (Previously Presented) A method as in claim 45 wherein the transistor includes a gate dielectric, a gate electrode, spacers and source/drain regions.

47. (Previously Presented) A method as in claim 45 wherein the detector includes a waveguide encapsulated by an oxide layer and at least one electrode.
48. (Previously Presented) A method as in claim 44 wherein the removing of the first substrate after the bonding includes one of a grind back process, an etching process, and an ion exfoliation process.
49. (Previously Presented) A method as in claim 44 wherein the removing of the first substrate after the bonding includes cleaving off the first substrate.